Q1 Github [1]

<https://github.com/aimeesimons/EEE3088F-Group-14.git>

Q2 Power Subsystem Failure Management [5]

In text, briefly describe what measures you’ve taken in your circuit design that will enable you to manage failures such as but not necessarily limited to: (i) component failure/destruction, (ii) trace damage, (iii) component shortage (if at PCB assembly time your component is no longer in stock), (iv) errors in your circuit design that are only detected post manufacture.

Q3 Sensing Subsystem Failure Management [5]

(i) component failure/destruction

(ii) trace damage

(iii) component shortage (if at PCB assembly time your component is no longer in stock)

(iv) errors in your circuit design that are only detected post manufacture.

Q4 Microcontroller interfacing Failure Management [5]

In text, briefly describe what measures you’ve taken in your circuit design that will enable you to manage failures such as but not necessarily limited to: (i) component failure/destruction, (ii) trace damage, (iii) component shortage (if at PCB assembly time your component is no longer in stock), (iv) errors in your circuit design that are only detected post manufacture.

Q5 Power Subsystem Schematic [10]

Q6 Sensing Subsystem Schematics [10]

Q7 Microcontroller Interfacing Schematic [10]

Q8 Planned ERCs [5]

Q9 Updated BOM [4]